	Name	M76P00	M73P00	AX58100	AX58200	AX58400	ET1100	ET1810/ET1811/ET1812	ET1815/ET1816/ET1817	ET1820/ET1821/ET182
	Туре	Dual-Core RISC-V SOC	Single-Core RISC-V SOC	ASIC	ARM MPU	Dual-Core ARM MPU	ASIC	Altera FPGA + IP Core	AMD (Xilinx) FPGA + IP Core	Microchip FPGA + IP Core
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of	Supplier	医应创科技 ArtInChip	医疝创科技 ArtinChip	ASIX	ASIX	ASIX	BECKHOFF	BECKHOFF	BECKHOFF	BECKHOFF
ETG and the EtherCAT licensor.	Supplier	Artinchip Guangdong Jiangxinchuang Technology	Artinchip Guangdong Jiangxinchuang Technology	ASIX Electronics Corporation	ASIX Electronics Corporation	ASIX Electronics Corporation	Beckhoff Automation	Beckhoff Automation	Beckhoff Automation	Beckhoff Automation
EtherCAT devices based on these chips can obtain a "Conformance Tested"	Package	BGA196, 0.8 mm pitch eLQFP144, 0.5 mm pitch BGA144, 0.8 mm pitch	eLQFP144, 0.5 mm pitch BGA144, 0.8 mm pitch	80-pin LQFP 0.4 mm pitch	144-pin HSFBGA 0.8 mm pitch	225LD EHS-TFBGA 0.8 mm pitch	BGA128 0.8 mm pitch	FPGA dependent	FPGA dependent	FPGA dependent
Using unauthorized chips may	Size	BGA196: 12X12 mm eLQFP144: 20x20 mm BGA144: 10x10 mm	eLQFP144,: 20x20 mm BGA144: 10x10 mm	12 x 12 mm	10 x 10 mm	13 x 13 mm	10 x 10 mm	FPGA dependent	FPGA dependent	FPGA dependent
lead to problems in the field. Licensees whose chips are released but not yet listed in this	μC Interface	μC bus (internal, AHB)	μC bus (internal, AHB)	SPI/parallel (8/16-bit, asynchronous)	uC bus (Internal, AHB)	uC bus (Internal, AHB)	serial/parallel (8/16bit, sync/async)*	serial/parallel (8- /16-/32-bit, async) AVALON®* or AMBA-AXI4- Interface	serial/parallel (8- /16-/32-bit, async) OPB®* and PLB®*or AMBA-AXI4- Interface	serial/parallel (8- /16-/32-bit, async) AMBA-AXI4-Interface
overview should contact info@ethercat.org	Digital I/O	-	-	32	-	20	8-64*	8-64*	8-64*	8-64*
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.	General Purpose I/O	-	-	32	up to 76*	up to 97*	0-32*	0-128*	0-128*	0-128*
Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	8 Kbyte	8 Kbyte	9 kByte	9 kByte	9 kByte	8 kByte	060 kByte*	060 kByte*	060 kByte*
their own purposes could violate the rights of the owners.	SyncManager Entities	8	8	8	8	8	8	016*	016*	016*
Note: Subject to technical	FMMU Entities	8	8	8	8	8	8	016*	016*	016*
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes(64 Bit)	yes(64 Bit)	yes (64-bit)	yes (64-bit)	yes (64-bit)	yes	yes*	yes*	yes*
information. The content of all	No. of Ports	2-3 (RMII/MII)	2 (RMII/MII)	2 (100BaseTX) + Opt. 1 (MII)	2 (100BaseTX) + Opt. 1 (MII)	2 (100BaseTX) + Opt. 1 (MII)	2-4 (MII/E-BUS)*	1-4 (MII/RMII/RGMII)	1-4 (MII/RMII/RGMII)	1-4 (MII/RMII/RGMII)
entries within the ESC overview is submitted by ETG members themselves. The ETG members are in charge of sales and support of their products as well as for the content of their entries. ETG therefore disclaims any liability for information contained therein.		FPU and DSP,1 MB on-chip SRAM, USB FS OTG, additional RMII/MII Ethernet MAC with IEEE1588,1xCordic,1xFFT,2xHCL, 1xPFM,1xDCE,4xGPT,2x14bit 2Msps 24CH ADC,4xPGA,24CH EPWM/HRPWM,6xCAP,1dxQEP, 2xQOUT,2xCPM,4xSDFM,1xPBU	1xPFM,1xDCE,4xGPT,2x14bit	100BASE-FX support 2 integrated PHYs 3-ch PWM and S/D I/F ABZ and Hall encoder I/F SPI master I/F	2 integrated Ethernet PHYs, USS 2.0 HS OTG, 10/120Mbps Ethernet MAC with RMII and hardware cryptography accelerator 6xLPUARTS, 3xISO-7816-3, 1xQuad-SPI, 3xI2C, 1xI2S, 2xUSCI, 2xCAN, 1xSPI Flash I/F, 2xSDHC, 1x416-ch/12-bit ADC, 2x12-bit DAC, 2xAnalog Comparators, 2xOperational Amplifiers, 4x32-bit timers, 2x416-bit PWM counters, 2xQEI 1xECAP, supports Real-Time Clock (RTC), Built-in Die Temperature Sensor (DTS)	Dual-Core 480MHz ARM Cortex-M VAT & 240MHz Cortex-M AUCU. 2 Mbytes embedded Flash memory, Z ESC Integrated PHY, USB HS OTG, Additional RMII/MII Ethernet MAC with IEEE 1588 for multiprotocol support, TFT-LCD display controller, Security and Cryptographic Accelerator, 96-bit UID, Watchdog, RTC /SysTick timers, Rich communication/control interfaces such as SPI/UART/IZC /IZS/SAI/CAM/SDMMC/ADC/DA C/HDMI-CEC/PWM/DFSDM, etc.	BGA routable with standard PCB	OpenCore Plus are available.	Various license models and evaluation Version are available. A wide range of Xilinx FPGAs are supported	estimated market release- quarter 2025 Various license models ar evaluation Version are available. A wide range of Microchi FPGAs are supported
	Further information	https://www.artinchip.com/p/32.html	https://www.artinchip.com/p/32.html	Mittee Flances and cores being introductified until all thermed 5 ther CATHACES 100	hitter illner asia con la imbedustini salatifihansa Ether ATAX5000	Misschese six con transconductindustricEthanesEthacATIXXS8600.	https://www.beckhoff.com/ET1100			

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s of July 2025										
	Name	ET1825/ET1826/ET1827	CF1103	CF1106	GD32H75E	GD32H77E	GDSCN832	Anybus NP40	netX 500	netX 51
	Туре	Lattice FPGA + IP Core	A4h	A4h	мси	мси	ASIC	ARM MPU	ASIC	ASIC
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of	Supplier	BECKHOFF	向码灵半导体 Codelar	向码灵半导体 Codelar Sent Ground	GigaDevice	GigaDevice	GigaDevice	Hms	hilscher enpowering communication	hilscher appowering communication
ETG and the EtherCAT licensor.	Supplier	Beckhoff Automation	Codefair Semiconductor Technology	Codefair Semiconductor Technology	GigaDevice	GigaDevice	GigaDevice	HMS Industrial Networks	Hilscher Gesellschaft für Systemautomation mbH	Hilscher Gesellschaft für Systemautomation mbH
EtherCAT devices based on these chips can obtain a "Conformance Tested" certificate.	Package	FPGA dependent	QFN88L/QFN100L	QFN64L/QFN88L	BGA240	BGA176, LQFP176, BGA100	QFN64	BGA VF400 0.8 mm pitch	BGA345 1 mm pitch	PBGA324 1 mm pitch
Using unauthorized chips may	Size	FPGA dependent	10mm x 10mm/12mm x 12mm	9mm X 9mm/10mm x 10mm	14 x 14 mm	10 x 10 mm, 26 x 26 mm, 8 x 8mm	9 x 9 mm	17 x 17 mm	22 x 22 mm	19 x 19 mm
Licensees whose chips are released but not yet listed in this	μC Interface	serial/parallel (8- /16-/32-bit, async) AMBA-AXI4-Interface	-	/8/16 bit μC interface	OSPI	OSPI/parallel (8/16-bit)	OSPI/parallel (8/16-bit)	Anybus interface (8- / 16-bit 30 ns parallel, 20 MHz SPI, Shift register, UART)	μC bus (internal, 32bit)	μC bus (internal, 32bit)
overview should contact info@ethercat.org	Digital I/O	8-64*	-	8bit/32bit	-		0-16	256 / 256 (Shift register mode)	-	-
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff	General Purpose I/O	0-128*	16bit	16bit	0-116	0-132	0-19	-	16	32
Automation GmbH, Germany. Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	060 kByte*	8KB	8KB	8 KB	8 KB	8 KB	12 kByte	256/512 Byte (Mailbox/Process Data)	6 kByte
their own purposes could violate the rights of the owners.	SyncManager Entities	016*	8	8	8	8	8	4	4	8
Note: Subject to technical	FMMU Entities	016*	8	8	8	8	8	4	3	8
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes*	64bit	64bit	yes (64 Bit)	yes (64 Bit)	yes (64 Bit)	yes	yes	yes
information. The content of all entries within the ESC overview is	No. of Ports		2	3	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX) + 1 (MII)	2 (MII)	2 (100BaseTX)	2 (100BaseTX)
submitted by ETG members are in charge of sales and support of their products as well as for the content of their entries. ETG therefore disclaims any liability for information contained therein. EtherCAT.	Specials	estimated market release 4th quarter 2025 Various license models and evaluation Version are available. A wide range of Lattice FPGAs are supported	Integrated MCU(Cortex-M3)	Integrated 2 100Mbps Ethernet PHYs	EtherCAT® SubDevice Controller integrated with Cortex®-M7 600MHz mircocontroller and dual ENET PHY 1207 DMPIS, 1MB SRAM, 4MB FLASH Math acceleration engine, EXMC I/F for FPGA/CPLD extension, HPDF for sigma-delta demodulation PWM, CAN-FD, USB, 100M ENET, rich analogs (14bit ADC, DAC, CMP) TFT-LCD I/F, Image Processing Accelerator, IECG1508 support, TJ 125C, advanced security	integrated with Cortex®-M7 600MHz mircocontroller and optional dual ENET PHY high performance embedded	Controller with dual integrated ENET PHY which contain a full duplex 100BASE-TX transceiver and support 100Mbps (100BASE TX) operation, supports HP Auto MDIX, allowing the use of direct connect or cross-over LAN cables.	Frame forwarding delay: 114 ns, MDP, possible to implement several device profiles	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-200MHz)	Multi-protocol support, Integrated PHYS, Integrated µC (ARM9-100MHz)
	Further information		http://www.codefairsemi.com/product-82239-207809.html	http://www.codefairsemi.com/product-62239-207809.html	tiles tinner stealmine contradiction which confurence mustic CDF or senses CDF		The free deales and continued the shifts and among much 1700s selected 50-7	www.anjbus.com/technologies/network_processors.shtml	https://www.hilscher.com/neb	https://www.hilscher.com/n
	Data Sheet	https://www.beckhoff.com/en-en/onduste/-o/et/encer-development-onduste/	Machine and Galanti conforms to be able to the accompany of the Conformation of	Machine and dissert conformal final harmonic and CONSTRUCTION CONTROL AND CONSTRUCTION CONTROL AND CONSTRUCTION CONTROL AND CO	Maximum stadence continuosite continuos estamente recutad COPT o servico COPT		You have assistance continued the which serfemence record (TAThe series of TATh	grava ambus considerationals MMAS 19% 25 Anabus N 20 Compact Contri 20 CH2 cell	the law their collections, study (18 normalist CON December 1998)	to be the section of

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EtherCAT SubDevice Controller (ESC) Overview

	Name	netX 52	netX 90	netX 100	HPM6E00	HPM5E00	XMC4300	XMC4800	LAN9252	LAN9253
	Туре	ASIC	ASIC	ASIC	RISC-V MPU	RISC-V MPU	ARM MPU	ARM MPU	ASIC	ASIC
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of ETG and the EtherCAT licensor.	Supplier	hilscher empowering communication	hilscher enpowering communication	hilscher angowering communication	HPMicro _{先值半导体}	PMicro _{先俄半导体}	infineon	infineon	MICROCHIP	MICROCHIP
	Supplier	Hilscher Gesellschaft für Systemautomation mbH	Hilscher Gesellschaft für Systemautomation mbH	Hilscher Gesellschaft für Systemautomation mbH	HPMicro Semiconductor	HPMicro Semiconductor	Infineon Technologies	Infineon Technologies	Microchip Technology Incorporated	Microchip Technology
EtherCAT devices based on these chips can obtain a "Conformance Tested"	Package	PBGA244 1 mm pitch	LFBGA144 0.8 mm pitch	BGA345 1 mm pitch	BGA289 (0.8mm pitch) BGA196 (0.8mm pitch)	BGA196 (0.8mm pitch) BGA121 (0.8mm pitch) eLQFP100 (0.5mm pitch)	100 LQFP (0.5 mm)	100 LQFP (0.5 mm)	64 pin QFN (0.5 mm pitch) 64 pin TQFP-EP (0.5 mm pitch)	64 pin QFN (0.5 mm pitc
Certificate. Using unauthorized chips may lead to problems in the field.	Size	15 x 15 mm	10 x 10 mm	22 x 22 mm	14 mm x 14 mm 12 mm x 12 mm	12 mm x 12 mm 9 mm x 9 mm 14 mm x 14 mm	16 x 16 mm	20 x 20 mm 16 x 16 mm 12 x 12 mm	9 x9 mm 12 x 12 mm	9 x9 mm
Licensees whose chips are released but not yet listed in this	μC Interface	μC bus (internal, 32bit)	μC bus (internal, 32bit)	μC bus (internal, 32bit)	200MHz μc bus (internal 64bit)	200MHz μc bus (internal 64bit)	μC bus (internal, AHB)	μC bus (internal, AHB)	Host Bus/SPI/SQI	8/16-bit Host Bus/SPI/S
overview should contact info@ethercat.org	Digital I/O	-	-	-	32	32	-	-	0-16*	0-16*
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff	General Purpose I/O	24	16	16	Up to 206	Up to 148	0 - 46	0 - 123	0-16*	0-16*
Automation GmbH, Germany. Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	6 kByte	6 kByte	256/512 Byte (Mailbox/Process Data)	60 kByte	60 kByte	8 kByte	8 kByte	4 kByte	8 kByte
their own purposes could violate the rights of the owners.	SyncManager Entities	8	8	4	8	8	8	8	4	8
Note: Subject to technical	FMMU Entities	8	8	3	8	8	8	8	3	8
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes	yes	yes	Yes	Yes	yes (64 Bit)	yes (64 Bit)	yes	yes
information. The content of all	No. of Ports	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX)	3 (MII/RMII/RGMII)	3 (MII/RMII/RGMII)	2 (MII)	2 (MII)	2 (100BaseTX) + opt. 1 (MII)	2 (100BaseTX) + opt. 1 (N
	Specials	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-100MHz)	Multi-protocol support, Integrated μC, OnChip Flash 1,5 Mbytes, OnChip DC-DC Converter, (ARM Cortex M4-100MHz) Additional integrated Application Controller (ARM Cortex M4 - 100 MHz)	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-200MHz)	600MHz Dual-Core RISC-V CPU 2MB SRAM/Opt 4 MB Flash 4-axis motor controll digital encoder interface (EnDat, BISS, others, etc) Multi-protocol support w/ 3- port 1Gpbs ENET TSN Switch USB HS OTG/CAN-FD UART/SPI/12C 4x 16b/2M5P5 ADC	480MHz RISC-V CPU 512KB SRAM/3 MB Flash 2-axis modror controll USB HS OTG/CAN-FD UART/SPI/I2C 2x 16b/2MSPS ADC	EtherCAT* node on an ARM* Cortex*-N4 processor with up to 256k9 no-chip flash, 128k8 on-chip RAM and analog/mixed signal capabilities. Qualified for up to 125°C ambient temperature.	EtherCAT® node on an ARM® Cortex®-M4 processor with up to 2MB on-chip flash, 352kB on- chip RAM and analog/mixed signal capabilities. Qualified for up to 125°C ambient temperature.	Cable Diagnostics, 100FX support, 2 integrated PHVS, integrated 1.2V regulator	Host EEPROM Emulatio support Supports for low-cost 25f crystal Cable Diagnostics, Wake on LAN, 2 integrated PHYs, Single Supply operation (3 Integrated 1.2V regulat
	Further information	https://www.hilscher.com/neb	https://www.hilscher.com/netx	https://www.hilscher.com/net/	Cabinari reference com broduct-center inicocontroller hamilia.	blics //www.homicro.com/product-center/microcontroller/hom5e/	www.infineon.com/ethercat	www.infineon.com/ethercat	https://www.microchip.com/en-us/product/LAN9252	https://www.microchip.com/en-us/product

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as of July 2025										
	Name	LAN9254	LAN9255	N32H765IxB7EC	N32H785XxB7EC	N32H765IxB7EC	N32H785XxB7EC	i.MX RT1180	EC-1	RZ/T1
	Туре	ASIC	ARM MCU	ARM MCU	ARM MCU	ARM MCU	ARM MCU	ARM MCU	ARM MPU	ARM MPU
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of	Supplier	MICROCHIP	MICROCHIP	Nation 😵	Nation 🗞	NSING	NSING	NXP	RENESAS	RENESAS
ETG and the EtherCAT licensor.	Supplier	Microchip Technology Incorporated	Microchip Technology Incorporated	Nations Technologies Inc	Nations Technologies Inc	NSING Technologies Pte	NSING Technologies Pte	NXP Semiconductors	Renesas Electronics Corporation	Renesas Electronics Corporation
EtherCAT devices based on these chips can obtain a "Conformance Tested" certificate.	Package	80 pin TQFP-EP (0.5 mm pitch)	128 pin TQFP (0.4 mm pitch)	UFBGA176+25 pitch 0.65mm	TFBGA240+25 pitch 0.8mm	UFBGA176+25 pitch 0.65mm	TFBGA240+25 pitch 0.8mm	289 pin MAPBGA (0.8 mm p.) 144 pin MAPBGA (0.8 mm p.)	196 pin BGA (0.8 mm)	FBGA320 0.8 mm pitch
Using unauthorized chips may	Size	12x12 mm	14x14 mm	10×10 mm	14×14 mm	10×10 mm	14×14 mm	14 x 14 mm 10 x10 mm	12 x 12 mm	17 x 17 mm
lead to problems in the field. Licensees whose chips are released but not yet listed in this	μC Interface	8/16-bit Host Bus/SPI/SQI	SPI/SQI up to 60MHz	μC bus (internal, AHB)	μC bus (internal, AHB)	μC bus (internal, AHB)	μC bus (internal, AHB)		USB Host/Function, CAN, SCIFA, I2C RSPI, Flash	16/32-bit parallel and various serial (SPI/I2C/UART)
overview should contact info@ethercat.org	Digital I/O	0-32*	0-32*	-	-	-	-		-	-
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff	General Purpose I/O	0-32*	0-32*	126 GPIOs	168 GPIOs	126 GPIOs	168 GPIOs		115* GPIOs / 8 Input (port multiplexed, partial 5V-tolerant, open drain, input pull-up)	0-209*
Automation GmbH, Germany. Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	8 kByte	8 kByte	8KB	8KB	8KB	8KB	8 kByte	512 KB (ATCM) with ECC 32 KB (BTCM) with ECC	8 kByte
their own purposes could violate the rights of the owners.	SyncManager Entities	8	8	8	8	8	8	8	8	8
Note: Subject to technical	FMMU Entities	8	8	8	8	8	8	8	8	8
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes	yes	yes (64 Bit)	yes (64 Bit)	yes (64 Bit)	yes (64 Bit)	yes	yes (64 bit)	yes
information. The content of all entries within the ESC overview is	No. of Ports	2 (100BaseTX) + opt. 1 (MII)	2 (100BaseTX) + opt. 1 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (RMII/MII)
submitted by ETG members themselves. The ETG members are in charge of sales and support of their products as well as for the content of their entries. ETG therefore disclaims any liability for information contained therein. EtherCAT.	Specials	Host EEPROM Emulation support Supports for low-cost 25MHz crystal Cable Diagnostics, Wake on LAN, 2 integrated PHYs, Single Supply operation (3.3V) Integrated 1.2V regulator	Integrated SAMESJI ARM Cortex-M4F MCU 1MB Progammable Flash 256KB Main Memory SRAM Extended Industrial Temperature rated (-40 to +105C) Cable Diagnostics, Wake on LAN, 2 integrated PHys, Single Supply operation (3.3V) Integrated 1.2V regulator		Dual-Core 600MHz ARM Cortex-M7 & 300MHz Cortex-M4 MCU, 2/4MB on-chip FLASH, 1504KB SRAM + 4KB Backup SRAM, 3DCS, 4 high-speed comparators, 6 DACs, integrated with multiple high-speed (US)ART, 12C, xSPI, SPI, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, Ethernet, supports digital camera interface (DVP), supports FITLCD graphical interface, JPEG hardware encoder/decoder, and GPU, built-in high-performance encryption algorithm hardware acceleration engine, supports AES/TDES, SHA, SMA algorithms, supports TRNG true random number generator, supports CRC8/16/32.	2/4MB on-chip FLASH, 1504KB SRAM + 4KB Backup RAM, 3 12 bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, integrated with multiple high-speed U(S)ART, 12C, xSPI, SPI, USBHS Dual Role, CAN-FD, SDRAM, FEMC, 5DMMC, Ethernet, supports digital camera interface (DVP), supports TFT-LCD graphical interface, JPEG hardware encoder/decoder, and GPU, built-in high-performance encryption algorithm hardware acceleration engine, supports	Dual-Core 600MHz ARM Cortex-M7 & 300MHz Cortex-M4 MCU, 2/4MB on-chip FLASH, 1504KB SRAM + 4KB Backup SRAM, 3 MCS, 4 high-speed comparators, 6 DACs, integrated with multiple high-speed (US)ART, 12C, xSPI, SPI, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, Ethernet, supports digital camera interface (DVP), supports FITLCD graphical interface, JPEG hardware encoder/decoder, and GPU, built-in high-performance encryption algorithm hardware acceleration engine, supports KS/TDES, SHA, SMA algorithms, supports TRNG true random number generator, supports CRC8/16/32.	Multi-protocol support 240 MHz ARM* Cortex*-M33 Core (RT1181) 240 MHz ARM* Cortex*-M33 Core plus 800 MHz ARM* Cortex*-M7	Safety Functions, Multi-Function Pin Controller	Additional Ethernet port (RMII/MII), 2-axis high-speed motion control support, digital encoder interfaces (EnDat, BISS, others), Multi-protocol support, security option, functional safety support, Cortex-R4F (450/600MHz), Cortex-M3 (150MHz) cores
	Further information	https://www.microchip.com/en-us/product/LAN9254	https://www.microchip.com/en-us/product/LAN9255	https://www.nationatech.com/product/general/v32h-in52h785eo	https://www.nationatech.com/product/general/n32h/n32h/185acc	Hips: Praing com. aglanoducti Generalicorlesen T.N.XXH M.SMSTEC/	Mice (Insing com approchact/General/ordesm7NS2H7Ricoc7EX)	https://www.nxp.com/products/i.MX-RT1180	www.renesas.com/en-eu/ec-1	www.renesas.eu/products/mpumcu/rz/index.
	Data Sheet			https://www.nationstech.com/support/dow/	https://www.nationstech.com/support/dow/	https://nsing.com.sg/api/dowffebefore?did=3003	https://nsing.com.sg/api/dowfilebefore?did=3005	https://www.msp.com/docs/en/data-sheet/MXRT1180EC.pdf	The first result on the extended above control of the The Table 1 and	www.renesas.eu/products/mpumou/tz/Documentation.j

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as of July 2025										
	Name	RZ/N2L	RZ/T2M	R-IN32M3-EC	RX72M	C2000™ (TMS320F28388D/S)	Sitara AMIC110 SoC	Sitara AM3357/9	Sitara AM4377/9	Sitara AM571xE
	Туре	ARM MPU	ARM MPU	ARM MPU	ARM MPU	TI C28x subsystem(s) with ARM Connectivity Manager	ARM MPU	ARM MPU	ARM MPU	ARM MPU
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of	Supplier	RENESAS	RENESAS	RENESAS	RENESAS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS
ETG and the EtherCAT licensor.	Supplier	Renesas Electronics Corporation	Renesas Electronics Corporation	Renesas Electronics Corporation	Renesas Electronics Corporation	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporate
EtherCAT devices based on these chips can obtain a "Conformance Tested" certificate.	Package	FBGA225, 0.8mm pitch FBGA121, 0.8mm pitch	FBGA320, 0.8mm pitch FBGA225, 0.8mm pitch	BGA324 1 mm pitch	LFBGA224, 0.8mm pitch LFBGA176, 0.8mm pitch LFQFP176, 0.5mm pitch LFQFP140, 0.5mm pitch LFQFP100, 0.5mm pitch	337 BGA 0.8mm pitch 176 QFP 0.5mm pitch	324-pin NFBGA 0.8mm pitch	324-pin NFBGA 0.8 mm pitch	491-pin NFBGA, 0.65mm pitch (0.8 mm effective routing)	760-pin FCBGA 0.8 mm pitch
Using unauthorized chips may	Size	13 x 13 mm 10 x 10 mm	17 x 17 mm 13 x 13 mm	19 x 19 mm	LFBGA176: 13 x 13 mm LFBGA176: 13 x 13 mm LFQFP176: 24 x 24 mm LFQFP144: 20 x 20 mm	16 x16 mm 26 x 26 mm	15x15mm	15 x 15 mm	17 x 17 mm	23 x 23 mm
lead to problems in the field. Licensees whose chips are released but not yet listed in this	μC Interface	USB Host/Function, CAN-FD, SPI SCI, DSMIF, I2C, xSPI, External BUS IF(SRAM/SDRAM/Host IF)	, USB Host/Function, CAN-FD, SPI, SCI, DSMIF, I2C, xSPI, External BUS IF(SRAM/SDRAM)	16/32-bit parallel (master/slave) and serial (SPI/I2C/UART)	USB, CAN, UART, SPI, I2C, SCI, QSPI	16-bit async PDI interface	200MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)
overview should contact info@ethercat.org	Digital I/O	-	-	-	44	N/A	8	8	8	8
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff	General Purpose I/O	0-134*	0-193*	0-96*	0-182*	32	>32	> 32	> 32	> 32
Automation GmbH, Germany. Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	8 kByte	8 kByte	8 kByte	8 kByte	16 kByte	8 kByte	8 kByte	28 kByte	28 kByte
their own purposes could violate the rights of the owners.	SyncManager Entities	8	8	8	8	8	8	8	8	8
Note: Subject to technical	FMMU Entities	8	8	8	8	8	8	8	8	8
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes	yes	yes	yes (64 bit)	yes	yes	yes	yes	yes
information. The content of all entries within the ESC overview is	No. of Ports		3 (RGMII/RMII/MII)	2 (100BaseTX)	2 (100BaseTX/MII/RMII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)
submitted by ETG members themselves. The ETG members are in charge of sales and support of their products as well as for the content of their entries. ETG therefore disclaims any liability for information contained therein. EtherCAT.	Specials	Multi-protocol support (EtherCAT, etc), Optimized for network companion chip (parallel bus slave, xSP Islave interface to connect external application CPU), One chip solution for various applications, Functional safety support, Cortex-R52 (400MHz) core	Multi-protocol support (EtherCAT, etc), Optimized for motor control (2-axis high-speed motion control support, digital encoder interfaces (EnDat, BiSS, others, etc.), Functional safety support, Cortex-R52 Dual (800MHz) cores	typical incl. 2 PHYs		EtherCAT slave enabled real- time controller. Up to 925 MIPS. Single or dual C28x + CLA control subsystems for real-time control loops. Arm based Connectivity Manager for communications and host control. On-chip flash, RAM, Ax 16-bit ADC, SDFM, 32-ch PWM, analog comparator subsystem, multiple communications ports, configurable logic block for CPLD/FPGA replacement and absolue encoder support.	memory (no external DDR	Industrial Communications Subsystem (PRU-ICSS) for multi-protocol support, Gigabit Switch, CAN, display, ARM Cortex-A8 (275MHz-1000MHz)	Multi-protocol support, Second PRU-ICSS for Motor control (EnDat, sigma delta filtering etc.). Gigabit Switch, CAN, Display subsystem, 20/30 graphics, Camera I/F, Optional secure boot, ARM Cortex-A9 (upto 1 GHz)	Dual Industrial Communication Subsystem (PRU-ICSS) for multi protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), Motor control (EnDat, sigma delta filtering), 2D/3D Graphics Display subsystem, Video acceleration, PCIe, SATA, Optional secure boot, ARM Cortex-A15 (upto 1.5GH2), 2x M4 cores, 1x C66x DSP core
	Further information	www.renesas.com/rzn2l	www.renesas.com/rzt2m	www.renesas.eu/automation		www.ti.com/product/tms320f28388d	www.ti.com/amic110	www.ti.com/AM335x	www.ti.com/AM437x	www.ti.com/product/AM571
	Data Sheet	https://www.renexas.com/us/en/document/dather/2/group-dateshee	Most have reness contains to current delication proce-delached	www.renesas.eu/r-in	years remarks com/document/dath/72m-croup-data/heat-ev/1117m-00548ft	www.ti.com/lit/gpn/tms320f28388d	http://www.6.com/product/AMIC110/datasheet	www.ti.com/lit/ds/symlink/am3359.pdf	www.ti.com/lit/ds/symlink/am4379.pdf	www.ti.com/lit/ds/symlink/am5718.pd

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as of July 2025										
	Name	Sitara AM572xE	Sitara AM65x SoC	Sitara AM64x SoC	Sitara AM243x SoC	Sitara AM263x SoC	TR8211	TR8253	ANTAIOS	TRITON
	Туре	ARM MPU	ARM MPU	ARM MPU	ARM MCU	ARM MCU	ASIC	ASIC	ARM MPU	ARM MPU
The ESC functionality of the chips listed in this overview has been developed with the support and authorization of	Supplier	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	TEXAS INSTRUMENTS	记 创權科技	回耀科技	YASKAWA	YASKAWA
ETG and the EtherCAT licensor.	Supplier	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporated	Texas Instruments Incorporated	Triductor Technology (Suzhou) Inc.	Triductor Technology (Suzhou)	Yaskawa Europe GmbH	Yaskawa Europe GmbH
EtherCAT devices based on these chips can obtain a "Conformance Tested"	Package	760-pin FCBGA 0.8 mm pitch	784-pin S-PBGA 0.8mm pitch	441-pin FCBGA 0.8mm pitch	441-pin FCBGA 0.8mm pitch / 293-pin FCCSP 0.5mm pitch via channel array	324-pin NFBGA 0.8mm pitch	TQFP-100, 14x14mm, 0.5pitch / TFBGA-128, 10x10mm, 0.8pitch	QFN-64, 9x9mm, 0.5pitch / LGA-64, 9x9mm, 0.5pitch	TFBGA-380 (0.65 mm pitch) TFBGA-385 (0.8 mm pitch)	FCBGA-784 (0.8 mm pitch)
certificate. Using unauthorized chips may	Size	23 x 23 mm	23mmx23mm	17.2mmx17.2mm	17.2mmx17.2mm / 11mmx11mm	15mmx15mm	TR8211: 14×14 mm TR8211K: 10×10 mm	TR8253: 9x9 mm TR8253L: 9x9 mm	15 mm x 15 mm 19 mm x 19 mm	23 mm x 23 mm
lead to problems in the field. Licensees whose chips are released but not yet listed in this	μC Interface	200 MHz interconnect (internal, 32bit)	250MHz interconnect (internal, 256bit)	250MHz interconnect (internal, 128bit)	250MHz interconnect (internal, 128bit), SPI (external)	200MHz interconnect (internal, 64bit)	SPI/SQI Slave HBI (8/16-bit Multiplexed/Indexed)	SPI/SQI Slave HBI (8/16-bit Multiplexed/Indexed)	SPI / QSPI / 16 Bit asynchronous interface	SPI / QSPI / 16 Bit asynchronou interface
overview should contact info@ethercat.org	Digital I/O	8	8	8	8	8	Aug 32	0-16	26Bits Input, 20Bits Output	32Bits Input, 22Bits Output
Trademarks and Patents EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff	General Purpose I/O	> 32	>32	>32	>32	>32	0-16	0-16	up to 32	up to 32
Automation GmbH, Germany. Other designations used in this publication may be trademarks whose use by third parties for	DPRAM	28 kByte	60 kByte	60 kByte	60 kByte	28 kByte	8 kByte	8 kByte	up to 64 kByte	up to 64 kByte
their own purposes could violate the rights of the owners.	SyncManager Entities	8	8	8	8	8	8	8	8	8
Note: Subject to technical	FMMU Entities	8	8	8	8	8	8	8	8	8
modifications; no responsibility is accepted for the accuracy of this	Distributed Clock Support	yes	yes	yes	yes	yes	yes (64-bit)	yes (64-bit)	yes (64 bit)	yes (64 bit)
information. The content of all entries within the ESC overview is	No. of Ports	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2-3 (MII)	2 (100BaseTX) + opt. 1 (MII)	2 (100BaseTX) or 2 (MII)	4 Gbit Ethernet port
submitted by ETG members themselves. The ETG members are in charge of sales and support of their products as well as for the content of their entries. ETG therefore disclaims any liability for information contained therein.		Dual Industrial Communications Subsystem (PRU-ICSS) for multi- protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), 2D/3D Graphics, Display subsystem, Video acceleration, PCIe, SATA, Optional secure boot, 2x ARM Cortex-A15 (upto 1.5 GHz), 2x M4 cores, 2x C66x DSP cores	on internal memory (no external DDR needed), 3x Gigabit Industrial Communications Subsystem (PRU_ICSSG) for multi-protocol support (up to 3 EtherCAT slave instances), PRU_ICSSG also supports Motor Control functionality (Encoder feedback such as Hiperface-DSI and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-A53 cores at 1.1GHz, 2x Cortex-R5F core at 400MHz with		on internal memory (no external DDR needed), Dual Gigabit Industrial Communications Subsystem (PRU_ICSSG) for multi-protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), PRU_ICSSG also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Detta filtering), up to 4 x Arm Cortex-R5F cores	memory, Industrial Communications Subsystem (PRU_ICSS), PRU_ICSS also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-RSF cores at 400MHz, 2MB on-chip SRAM	external MCU,	Bullt-in 100Mbps fast Ethernet PHYS (Support for automatic detection and switching of cross lines i.e. HP Auto MDIX), 25MHz clock output for external MCU, LED polarity and EEPROM size configuration supported, Single Supply operation (3.3V)	2 x integrated PHYs, 1 x integrated GBit Ethernet MAC, Integrated ARM® Cortex®	Multi fieldbus protocol support, port Real-Time Ethernet switch wi integrated PHYs, with integrated PHYs, 2. integrated ABM* Cortex**A17 (1.266Hz), Secure Core, Backplan communication: SiceBus master for profichig's SNAP+ ASIC, Integrate technology module (2.SI/1 AzWY) / 4xCounter), QuadSPI interface (e.g. NOR Flash for firmware), DOF external memory interface, 25 CExpress* Controller, Other extern interfaces: 35 DYMMC, NAND, USS device, SRAM master/slave.
	Further information	www.ti.com/product/AM5728	www.ti.com/product/am6548	www.ti.com/product/am6442	www.ti.com/product/am2434	www.ti.com/product/am2634	https://www.triductor.com/product-5.html	https://www.triductor.com/product-5.html	The Pears serious as common describing and administration of the serious and t	The lines and so as control of the first and other first and of the lines and the line
	Data Sheet	www.ti.com/lit/ds/symlink/am5728.pdf	http://www.ti.com/product/am6548/datasheet	http://www.ti.com/product/am6442/datasheet	http://www.ti.com/product/am2434/datasheet	http://www.ti.com/product/am2634/datasheet	https://www.triductor.com/product-5.html	https://www.triductor.com/product-5.html	ettes illenen vaskanna eu cominnodustationifichioloonidustidetaliipoodustiantaine. 93	i https://www.vankawa.eu.com/orad.uste/profit/bio/broductivital/broductiviton.id

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